504P0068**30

FIG. 1


```
HOST
COMPUTER              2

                    BUFFER
                    MEMORY            5

         4                                6              7           11A~11D

                               CODE          RECORDING
3                              GENERATING    CONTROL
                               CIRCUIT       CIRCUIT

I/F      MEMORY
         CONTROLLER

                               ERROR        REPRODUCTION
                               CORRECTING   CONTROL
                               CIRCUIT       CIRCUIT

                                  9            8         21A~21H

                                  1
```
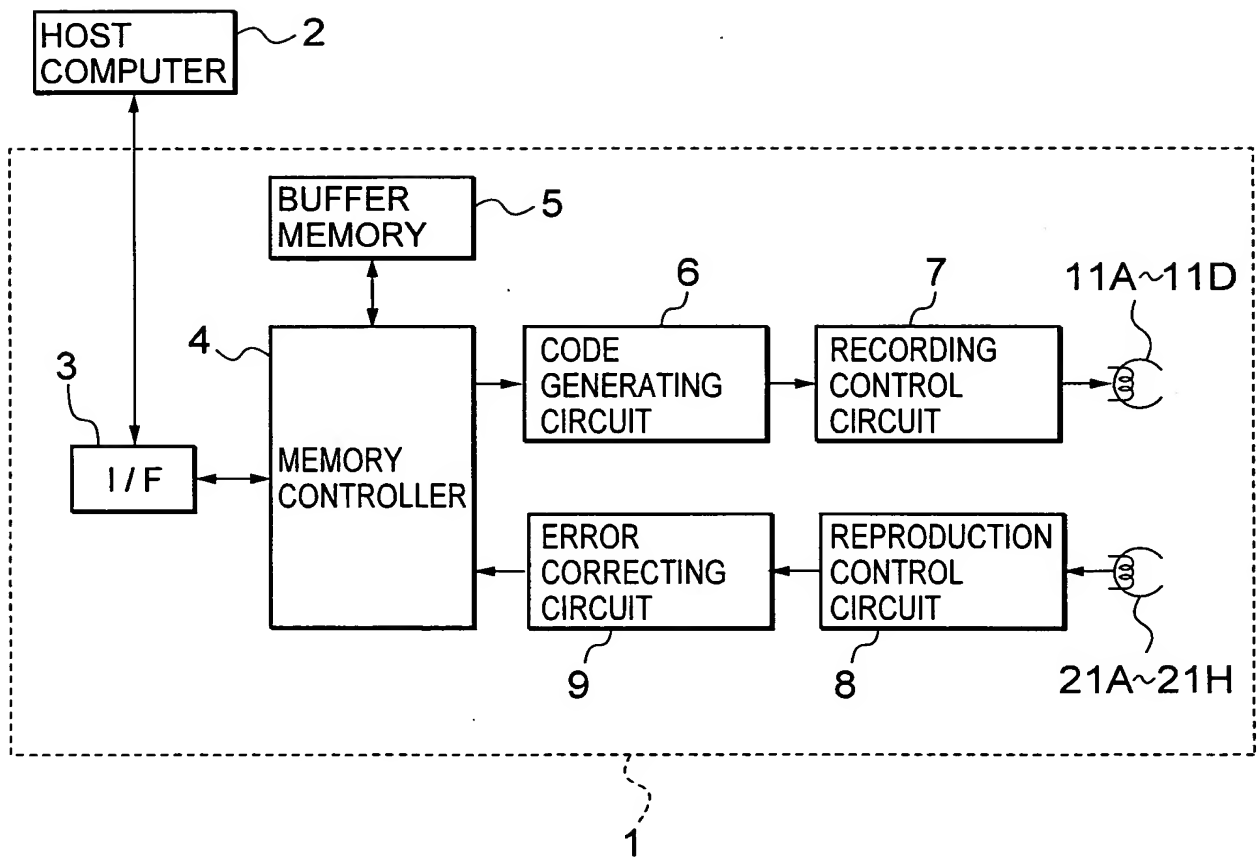
FIG. 2
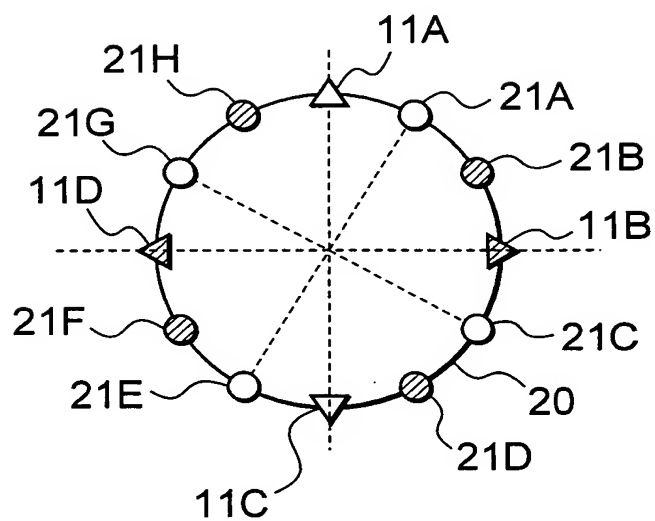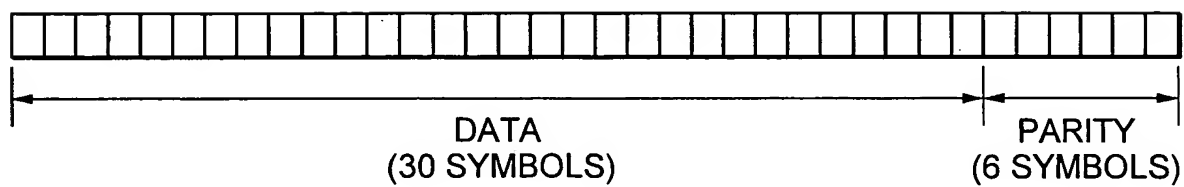

FIG. 3

DATA
(30 SYMBOLS)

PARITY
(6 SYMBOLS)

CODE (36, 30, 7)

36 : NUMBER OF SYMBOLS IN CODE

30 : NUMBER OF DATA SYMBOLS

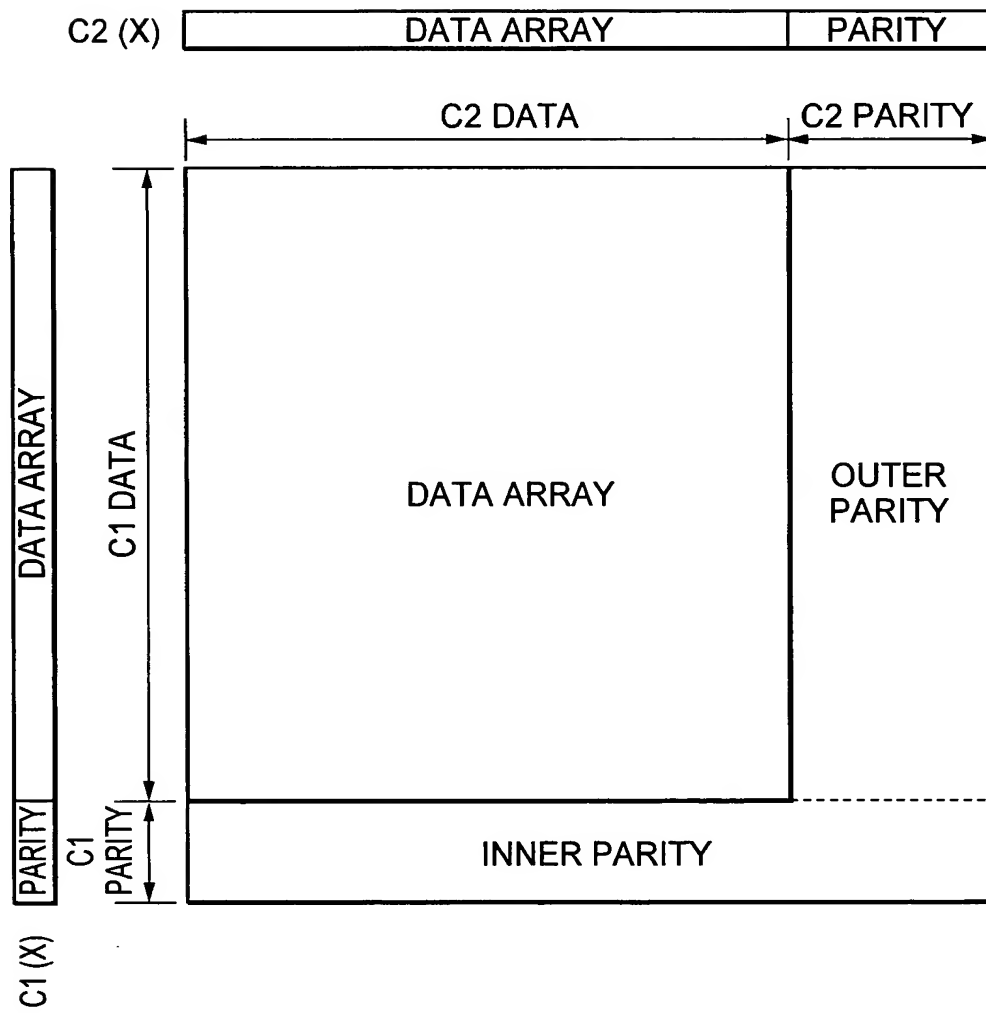 7 : MINIMUM DISTANCE BETWEEN CODES

CODE STRUCTURE EXAMPLE

FIG. 4

C2 (X)

DATA ARRAY	PARITY

FIG. 5

C1 DATA 240 BYTES / **C1 PARITY 16 BYTES** (vertical, left side)

	C2 DATA 192 BYTES						C2 PARITY 64 BYTES		
D0.0	D1.0	D63.0	D64.0	D127.0	D128.0	D191.0	Q192.0	Q254.0	Q255.0
D0.1	D1.1	D63.1	D64.1	D127.1	D128.1	D191.1	Q192.1	Q254.1	Q255.1
D0.2	D1.2	D63.2	D64.2	D127.2	D128.2	D191.2	Q192.2	Q254.2	Q255.2
D0.3	D1.3	D63.3	D64.3	D127.3	D128.3	D191.3	Q192.3	Q254.3	Q255.3
D0.4	D1.4	D63.4	D64.4	D127.4	D128.4	D191.4	Q192.4	Q254.4	Q255.4
D0.5	D1.5	D63.5	D64.5	D127.5	D128.5	D191.5	Q192.5	Q254.5	Q255.5
D0.6	D1.6	D63.6	D64.6	D127.6	D128.6	D191.6	Q192.6	Q254.6	Q255.6
D0.7	D1.7	D63.7	D64.7	D127.7	D128.7	D191.7	Q192.7	Q254.7	Q255.7
D0.232	D1.232	D63.232	D64.232	D127.232	D128.232	D191.232	Q192.232	Q254.232	Q255.232
D0.233	D1.233	D63.233	D64.233	D127.233	D128.233	D191.233	Q192.233	Q254.233	Q255.233
D0.234	D1.234	D63.234	D64.234	D127.234	D128.234	D191.234	Q192.234	Q254.234	Q255.234
D0.235	D1.235	D63.235	D64.235	D127.235	D128.235	D191.235	Q192.235	Q254.235	Q255.235
D0.236	D1.236	D63.236	D64.236	D127.236	D128.236	D191.236	Q192.236	Q254.236	Q255.236
D0.237	D1.237	D63.237	D64.237	D127.237	D128.237	D191.237	Q192.237	Q254.237	Q255.237
D0.238	D1.238	D63.238	D64.238	D127.238	D128.238	D191.238	Q192.238	Q254.238	Q255.238
D0.239	D1.239	D63.239	D64.239	D127.239	D128.239	D191.239	Q192.239	Q254.239	Q255.239
P0.240	P1.240	P63.240	P64.240	P127.240	P128.240	P191.240	Q192.240	Q254.240	Q255.240
P0.241	P1.241	P63.241	P64.241	P127.241	P128.241	P191.241	Q192.241	Q254.241	Q255.241
P0.254	P1.254	P63.254	P64.254	P127.254	P128.254	P191.254	Q192.254	Q254.254	Q255.254
P0.255	P1.255	P63.255	P64.255	P127.255	P128.255	P191.255	Q192.255	Q254.255	Q255.255
C1 (0) C1 (1) ··· C1 (63)			C1 (64) ··· C1 (127)			C1 (128) ··· C1 (191)	C1 (192) ··· C1 (254) C1 (255)		
DATA WRITTEN BY RECORDING HEAD 11A			DATA WRITTEN BY RECORDING HEAD 11B			DATA WRITTEN BY RECORDING HEAD 11C	DATA WRITTEN BY RECORDING HEAD 11D		

TWO-DIMENSIONAL ORTHOGONAL CODE OF C1 (256, 240, 17) $\times$ C2 (256, 192, 65)

TOTAL NUMBER OF WORDS : 65536 (256$\times$256), NUMBER OF DATA WORDS : 46080 (240$\times$192), REDUNDANCY RATE : 29.7%
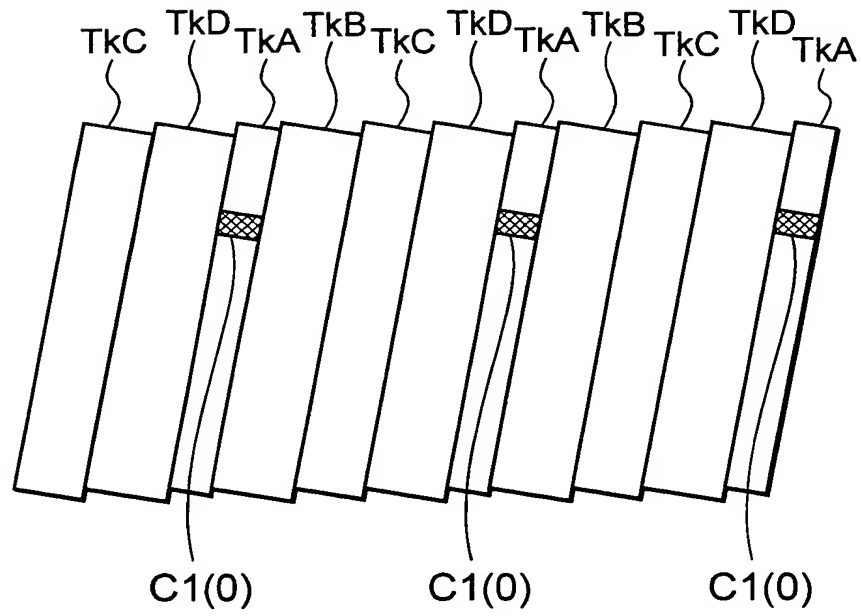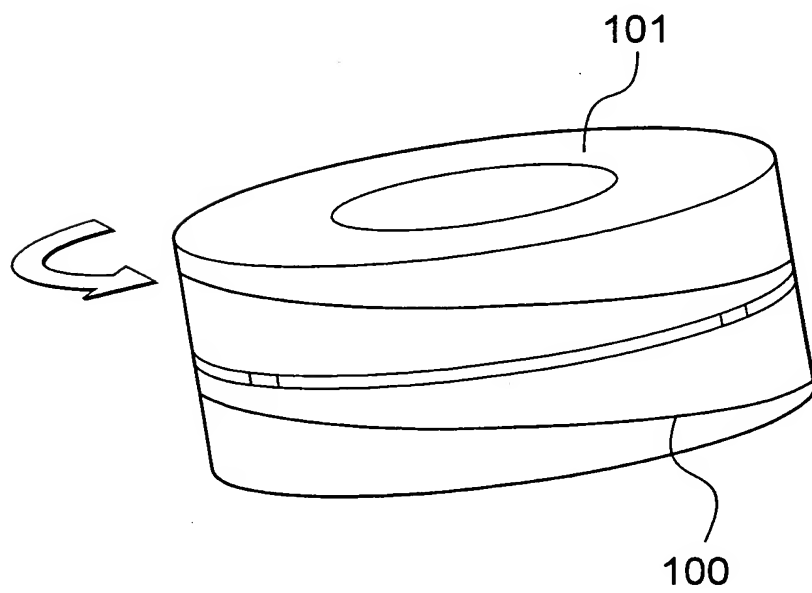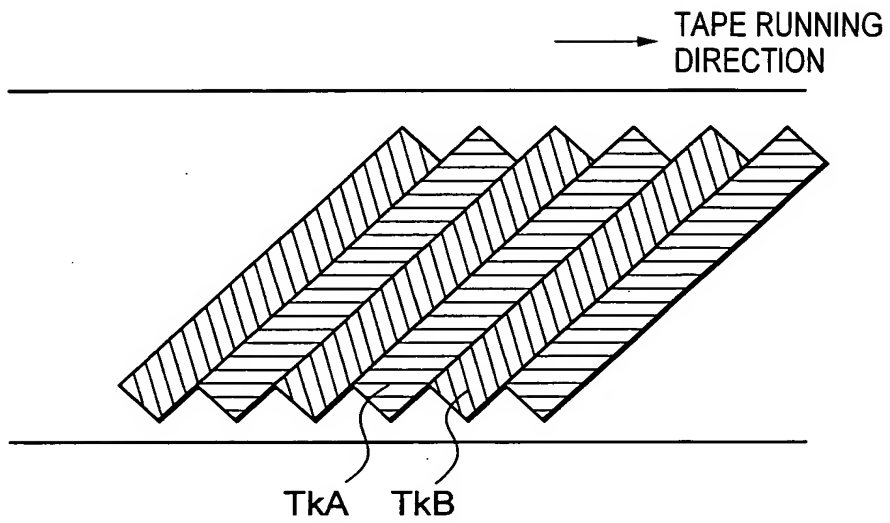
FIG. 6

TkC TkD TkA TkB TkC TkD TkA TkB TkC TkD TkA

C1(0)   C1(0)   C1(0)

FIG. 7

101

100

FIG. 8

TAPE RUNNING
DIRECTION

TkA   TkB

FIG. 9

TkA   TkB   TkA   TkB

102A

102B

102A

102B

A

B

A

B

FIG. 10

Tk

102

RUNNING TRAJECTORY
OF HEAD

FIG. 11

TkB

TkA-2   TkA-1

A   103

A   104

A   105

A   106

FIG. 12

TkA   TkB   TkA   TkB   TkA

A11

A12

P0

FIG. 13

TkA   TkB   TkA   TkB   TkA

A12(A11)

A11
(A12)

P1
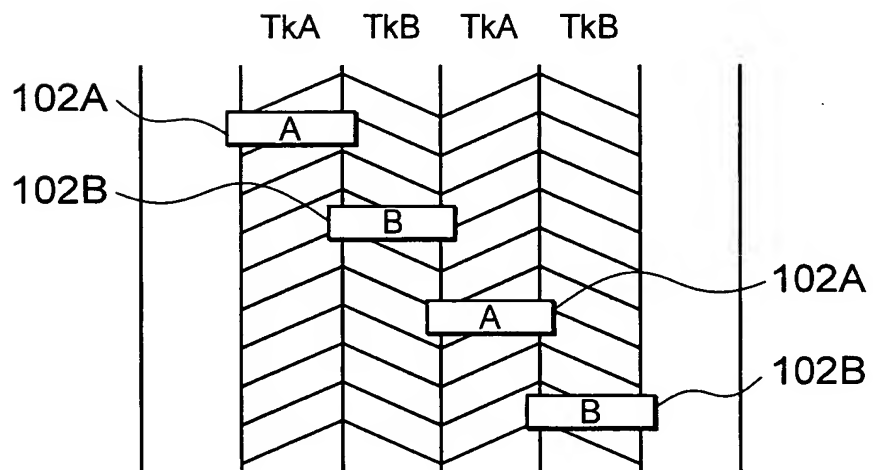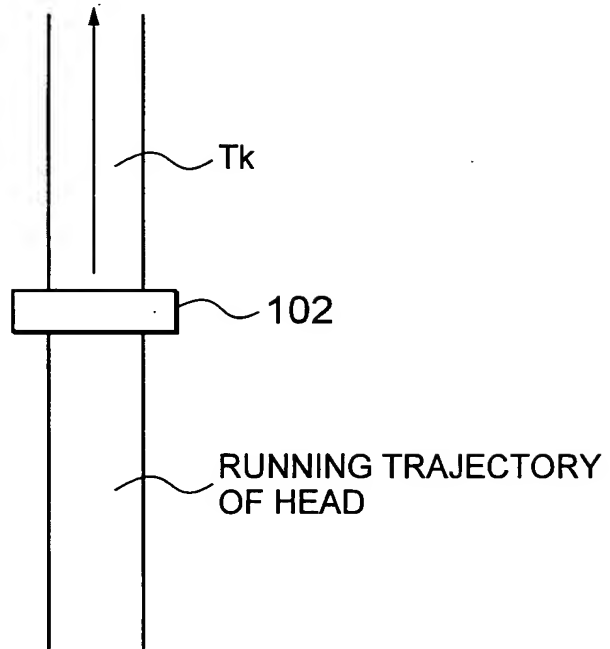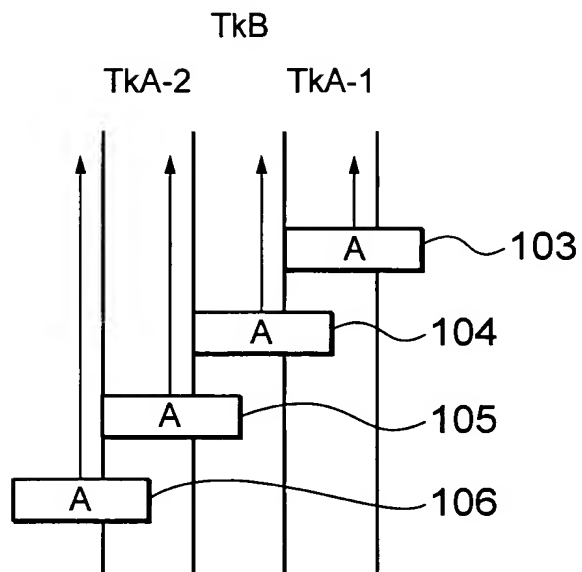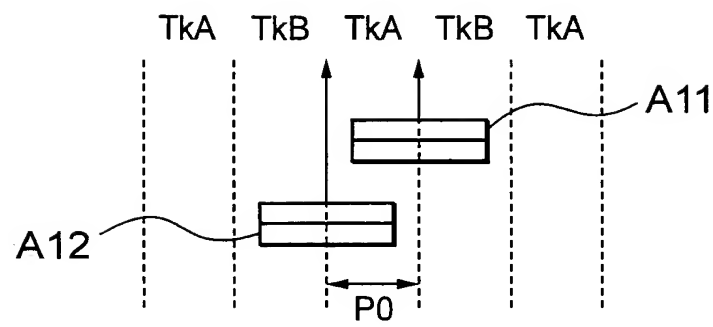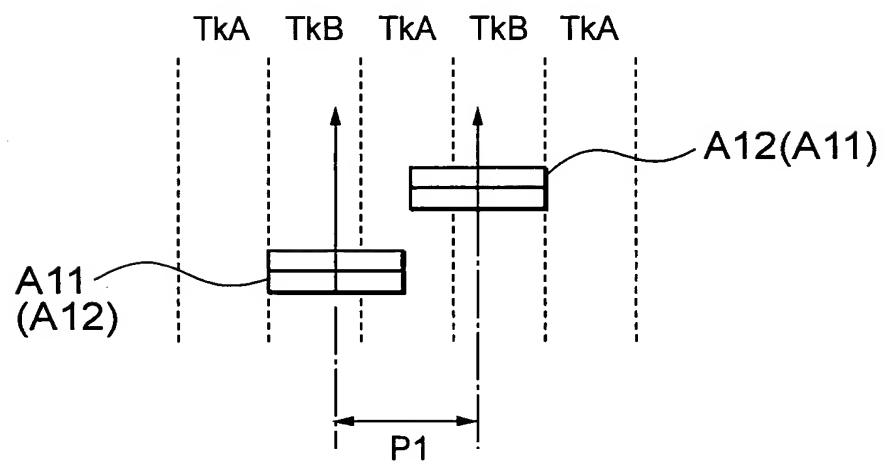
WITH ERROR

FIG. 14
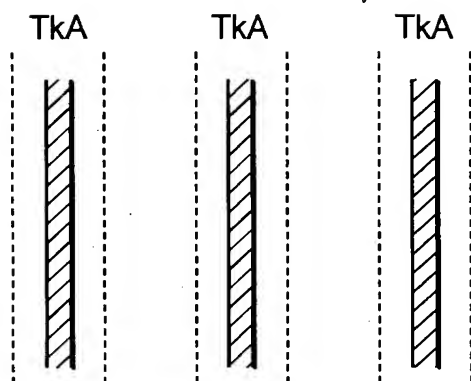
RECORDING BY ONE RECORDING HEAD PER AZIMUTH TRACK

FIG. 15
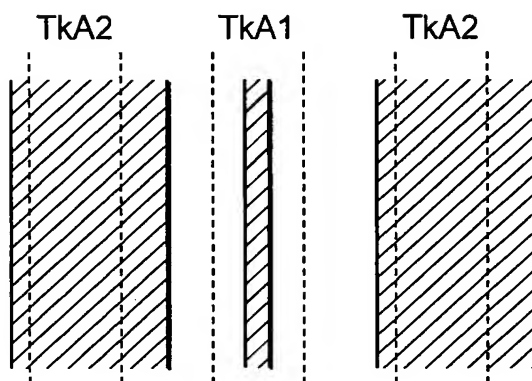
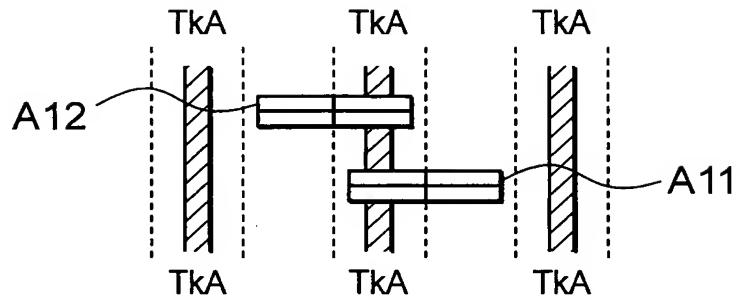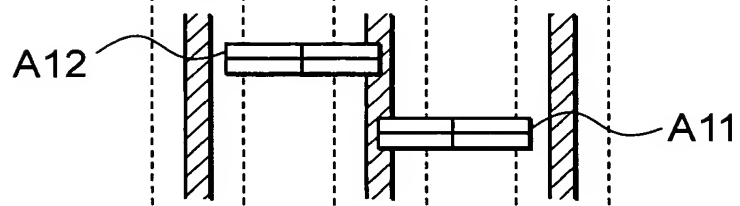RECORDING BY TWO RECORDING HEADS PER AZIMUTH TRACK
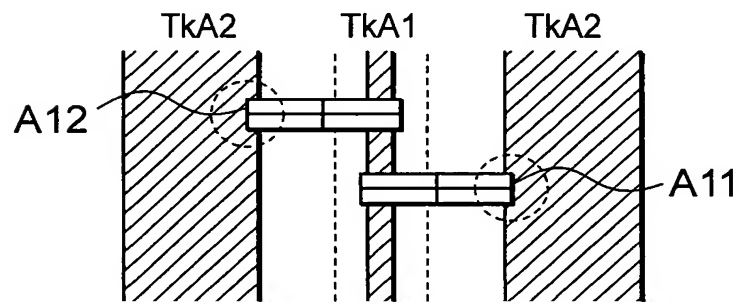
FIG. 16A
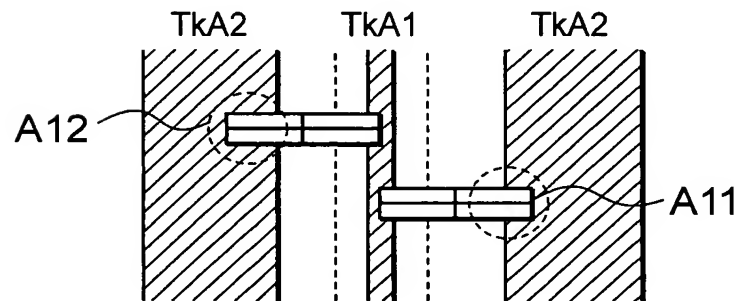

FIG. 16B

ONE-HEAD-PER-AZIMUTH-TRACK RECORDING

FIG. 17A

FIG. 17B

TWO-HEAD-PER-AZIMUTH-TRACK RECORDING